PVP 12

Code: **ECMC2T6C**

I M.Tech - II Semester - Regular Examinations – AUGUST 2016

DSP PROCESSORS AND ARCHITECTURE
(MICROWAVE & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Answer any FIVE questions. All questions carry equal marks

1. a) Show that computational complexity of FFT is faster than direct calculation of DFT. 7 M

b) For the filter
$y(n)=[-3x(n)+12\,x(n-1)+17\,x(n-2)+12\,x(n-3)-3x(n-4)]/35.$
Obtain the plot of 7 M
i) Magnitude
ii) dB magnitude
iii) Phase & group delay response for the filter.

2. a) Explain various number formats for representation signals and coefficients, consisting of the fixed point, floating point, double-precision and block floating point formats. 7 M

b) Explain the methods of estimating DSP computational errors. 7 M

3. a) Explain about DSP computational building blocks. 7 M

b) Explain in detail about programmability and program execution of DSP devices. 7 M

4. a) Explain the following terms in Pipelining: 7 M
i) Interlocking ii) Branching effects

b) Explain the role of interrupts during execution process in DSP processors. 7 M

5. a) Draw the functional diagram of the central processing unit of the TMS 320C54XX processors. 7 M

b) Explain various pipeline programming models. What is their influence on DSP operations? 7 M

6. a) Implement DSP algorithm for PID controller. 7 M

b) What is the advantage of FIR filter over IIR Filter? And implement the digital FIR low pass filter using the Parks-McClellan algorithm with the following Specifications. 7M
i) p=0.2 Rp=0.25 dB
ii) s=0.3 A_s=50 dB

7. a) With a neat structure, explain an 8 point DITFFT implementation on TMS320C54XX. 7 M

b) Explain about interpolation filters in DSP systems. 7 M

8. a) What is the address for the PCR register of McBSP2? Write instruction sequence to write it to data defined by PCR_VAL. 7 M

b) Design a data memory system with the address range 00800H-00FFFH for a C5416 processor. Use 2Kx 8 SRAM memory chips and draw its scheme. 7 M